What is claimed is:

1. A memory module recovery method for use with a memory module which comprises a volatile memory and a non-volatile memory for recovering said volatile memory when determined as defective in an electric test, said method comprising the steps of:

previously storing a defective row address and a defective column address corresponding to a memory cell of said volatile memory determined as defective, and defective device information for discriminating said volatile memory determined as defective in said non-volatile memory;

transferring said defective row address, said defective column address and said defective device information stored in said non-volatile memory to said volatile memory upon start-up of a system which is equipped with said memory module;

holding said transferred defective row address, defective column address and defective device information in said volatile memory; and

accessing a redundant memory cell instead of said memory cell determined as defective when said memory module receives an address corresponding to said memory cell based on said defective row address, said defective column address and said defective device information held

in said volatile memory.

2. The memory module recovery method according to claim 1, wherein:

said volatile memory comprises a plurality of fuse elements which can be blown out by laser light, said fuse elements being capable of holding information required to access said redundant memory cell instead of a memory cell determined as defective in a test at the end of a wafer manufacturing process.

3. A memory module comprising:

a non-volatile memory for storing a defective row address and a defective column address corresponding to a memory cell in a volatile memory which is determined as defective in an electric test; and

a volatile memory for holding said defective row address, said defective column address and said defective device information transferred thereto upon start-up of a system, said volatile memory including a redundant memory cell which is accessed instead of said memory cell determined as defective in said volatile memory when said memory module receives an address signal corresponding to said memory cell determined as defective.

4. The memory module according to claim 3, wherein:

said volatile memory comprises a plurality of fuse elements which can be blown out by laser light, said fuse elements being capable of holding information required to access said redundant memory cell instead of a memory cell determined as defective in a test at the end of a wafer manufacturing process.

5. A volatile memory having a redundant memory cell which is accessed instead of a defective memory cell in which a defect is found, said volatile memory comprising:

a defect information storage circuit for holding a defective row address and a defective column address transferred from the outside;

a device information storage circuit for determining whether or not said defective device information relates to said volatile memory itself to hold the result of the determination;

a row address comparator for comparing the defective row address stored in said defective information storage circuit with a row address supplied from the outside;

a column address comparator for comparing the defective column address stored in said defective information storage circuit with a column address supplied from the outside;

a redundant row decoder for activating a word

line connected to said redundant memory cell when said defective row address matches said row address to enable an access to said redundant memory cell; and

a redundant column decoder for activating a bit line connected to said redundant memory cell when said defective column address matches said column address to enable an access to said redundant memory cell.

6. The volatile memory according to claim 5, wherein:

said redundant row decoder and said redundant column decoder each include a plurality of fuse elements which can be blown out by laser light for holding information required to access said redundant memory cell instead of a memory cell which is determined as defective in a test at the end of a wafer manufacturing process.